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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,229	06/24/2003	Shih-Wei Wang	TS02-695	8541

7590 12/15/2004

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,229	WANG, SHIH-WEI	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated November 19, 2004, Applicant has elected Group I, claims **1-10**, drawn to a device, and canceled claims **11-25** is acknowledged. Accordingly, claims **1-10** are currently pending in this application.

Information Disclosure Statement

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim **1** is rejected under 35 U.S.C. 102(a, e) as being anticipated by Ni (USP: 6,563,166).

Regarding claim **1**, Ni discloses in Fig. 2A and the corresponding texts as set forth in column 3-line 65-column 4, line 67, a dual-bit split gate flash memory 100 comprises:

a plurality of memory cells 102a, 102b wherein each memory cell comprises:

a select gate 116a, 116b overlying a substrate 108 and isolated from said substrate by a select gate oxide layer 114a, 114b;

a first and second floating gate 130a, 130b, 148a, 148b on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer 126a, 126b, 128a, 128b ; and

a control gate 106 overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layers 154; and

source 124 and drain regions 140a, 140b within said substrate and shared by adjacent said memory cells.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim **2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ni (USP: 6,563,166) in view of Fulford et al. (USP: 6,040,602 hereinafter referred to as "Fulford").

Ni discloses the claimed limitations as above except for a channel length under said select gate and said first and second floating gates in between about 0.05 and 0.07 microns in 0. 18 micron technology. Fulford teaches in Fig. 1F that a shorter channel length results in a faster-performance transistor. Desirably, the channel length 132 is between 0.05 micron and 0.2 micron as set forth in col. 4, lines 37-40. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the channel length between about 0.05 and 0.07 microns in order to achieve a faster-performance transistor. Also, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the channel length between about 0.05 and 0.07 microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims **3-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ni (USP: 6,563,166) in view of Liang et al. (USP: 6,281,545 hereinafter referred to as "Liang").

Ni discloses the claimed limitations as above and said select gate comprises a polysilicon layer (col. 8, lines 8-10) except for said select gate has a thickness of between about 1000 and 1200 Angstroms; and a dielectric capping layer having a thickness of between about 800 and

1000 Angstroms; and wherein said dielectric capping layer comprises high temperature oxide. Liang teaches in 7 that a split-gate, flash memory cell comprises a dioxide dielectric cap layer 23 and said dielectric capping layer comprises high temperature oxide (col. 4, lines 39-46). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a dioxide dielectric cap layer 23 and said dielectric capping layer comprises high temperature oxide, as taught by Liang in order to protect the device. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the select gate has a thickness of between about 1000 and 1200 Angstroms; and a dielectric capping layer having a thickness of between about 800 and 1000 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims **5-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ni (USP: 6,563,166).

Ni discloses the claimed limitations as above and said oxide spacer comprises high temperature oxide (col. 7, lines 10-15), first and second floating gates are isolated from said substrate by a tunneling oxide 134a, 134b, said control gate comprises polysilicon (col. 8, lines 17-20), and said dielectric layer comprises a first layer of high temperature oxide, a second layer of silicon nitride, and a third layer of high temperature oxide (col. 7, lines 10-15) except for said select gate oxide has a thickness of between about 29 and 35 Angstroms, and said oxide spacer has a width of between about 400 and 500 Angstroms, a tunneling oxide having a thickness of

between about 80 and 100 Angstroms, wherein said first and second floating gates have a thickness of between about 1300 and 1600 Angstroms and a length of between about 500 and 700 Angstroms, said control gate having a thickness of between about 2000 and 2400 Angstroms, and the dielectric layer comprises a first layer of high temperature oxide, a second layer of silicon nitride, and a third layer of high temperature oxide, each layer having a thickness of between about 60 and 70 Angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form said select gate oxide has a thickness of between about 29 and 35 Angstroms, and said oxide spacer has a width of between about 400 and 500 Angstroms, a tunneling oxide having a thickness of between about 80 and 100 Angstroms, wherein said first and second floating gates have a thickness of between about 1300 and 1600 Angstroms and a length of between about 500 and 700 Angstroms, said control gate having a thickness of between about 2000 and 2400 Angstroms and the dielectric layer comprises a first layer of high temperature oxide, a second layer of silicon nitride, and a third layer of high temperature oxide, each layer having a thickness of between about 60 and 70 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

Andy Huynh

12/13/04

Patent Examiner